

APPLICATION
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TITLE: FRAME SHUTTER PIXEL WITH AN ISOLATED
STORAGE NODE

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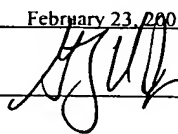
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FRAME SHUTTER PIXEL WITH AN ISOLATED STORAGE NODE

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This invention claims priority under 35 U.S.C. 119/120 from provisional application serial number 60/184,501 filed February 23, 2000.

BACKGROUND

[0002] CMOS active pixel image sensors may be operated using a "rolling" shutter. Such a shutter operates by reading out each row of pixels, and then resetting that individual row, and then rolling to read and then reset the next row of pixels. Each pixel hence gets read and then reset at slightly different times. Hence, each pixel has a slightly different time of integration. Some applications, such as high-speed photography, may require more time consistency than is possible using this approach. Therefore, in these other applications, a frame shutter may be used. In the frame shutter mode, all pixels in the array have substantially identical integration start times and integration stop times.

[0003] A frame shutter technique, using a photogate pixel with two transfer gates, is shown in Figure 1. A bridge diffusion isolates the photogate PG from the floating diffusion sense node (FD). Hence the charge in the photogate may be

integrated and reset independently. The charge is stored in a storage node 110, which may also be independently reset. Bridge diffusion BD2 isolates the photogate from the storage node. A second bridge diffusion BD1 isolates the photogate collection area from a reset level Vaa. The charge level in the photogate collection area 100 may be transferred to a storage node 110 via transfer gate 105.

[0004] This isolation allows the integration regions of all the photogates in the entire array to be clocked globally. The same timing therefore exists for each of the plurality of pixels in the array. Moreover, the charge is preserved until the desired time of readout. This enables the active pixel sensor can be read out row by row, thereby allowing the same readout structure as is currently used.

SUMMARY

[0005] The present application teaches a new structure which isolates the storage node in order to provide a better image quality in the resultant structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] These and other aspects will now be described in detail with reference to the accompanying drawings, wherein:

[0007] Figure 1 shows a traditional photogate frame shutter;

[0008] Figure 2A and 2B shows a first frame shutter with an isolated storage node with a photodiode;

[0009] Figure 3 shows a second frame shutter with an isolated storage node using a photogate; and

[0010] Figure 4 shows an dual well embodiment.

DETAILED DESCRIPTION

[0011] The present inventors have recognized that a problem may occur with the conventional technique shown in Figure 1. This problem may result from charge collection by the storage node 110. The storage node 110 may itself behave like a small photodiode. As such, the storage node 110 may collect some of the charge which is not collected by the photogate 100. This charge may be collected during the entire storage and/or readout time. This integration uses the rolling shutter type, providing a different readout period for each row of pixels. Hence, the entire storage time may typically be much longer than the desired frame shutter integration time. This leakage may correspond to image smear, and also may become more severe as the photogate size is reduced to make smaller pixel sizes.

[0012] According to the present system, embodiments of which are disclosed herein, the storage node is placed inside a protected area. For example, the storage node, which is the node that stores the photoelectrically induced signal, i.e. the

charge from the photoreceptor after the charge integration time, may be placed inside an N type well that is protected by a light shield, e.g., a metal light shield. The shield has the effect of preventing a light induced signal from effecting the amount of charge stored in the storage node. The shield may prevent photons from converting into a photoelectric signal such as charge within the N well.

[0013] Any charge that is generated in the other regions of the pixel that diffuses to the N well boundary, will be swept into the well contact and hence will never reach the storage node. Of course, small leakage signals may still exist. The signals result primarily from photons which reach the N well as a result of multiple reflections. This is substantially reduced as compared with the kind of conventional system.

[0014] Figures 2A show a first embodiment. Figure 2A shows a well view of the embodiment, while figure 2B shows a transistor level circuit for this embodiment. The pixel in Figure 2A shown while integrating, with both the photoreceptor 200 and floating diffusion sense node FD having been reset. The storage well 220 is still at its reset level; that is the level V_{rst} , as in the reset well 232.

[0015] N-well 210 isolates the wells, including storage well 220, from the receptor, here photodiode 200, in the substrate. The isolated wells may include reset diffusions 232, 234. The

diffusion 234 is a photodiode reset, actuated via NMOS transistor 225. The floating diffusion reset well 232 is actuated via PMOS transistor 230.

[0016] The photodiode 200 may be a standard n type photodiode. This is electrically connected via 202 to a P-type bridge diffusion node 205 within n type well 210. The bridge diffusion receives charge from the photodiode.

[0017] The photodiode may be reset by lowering the voltage on the gate 215. This forces both the photodiode and bridge diffusion node 205 to the voltage V_{rst} . When the reset is removed, the photodiode 200 begins to integrate the incoming photoelectric signal. This reduces the voltage on both the photodiode 200, and the connected bridge diffusion node 205.

[0018] At the end of the integration period, the signal on the photodiode and bridge diffusion well 205 is sampled onto the storage type P node 220, by lowering the voltage on the sampling gate 225. The charge is transferred from the photodiode to the storage node in proportion to its relative capacitance. Later, the sample gate 225 is released, and the storage node 220 becomes isolated from any photoelectric current in bridge diffusion 205 by the sample gate 225. The storage node 220 is also isolated from photoelectric current in the substrate by the N well.

[0019] The stored value in the storage node 220 is read out in the traditional method of CMOS active pixel sensor read out.

[0020] After readout, the storage node 220 is reset to the reset value V_{rst} in well 232, using the reset memory gate 230. The stored voltage will be:

$$V_{stored} = V_{rst} - \frac{Q_{photons}}{C_{storage} + C_{bridge} + C_{pd}}$$

[0021] The conversion gain is based on the ratio of the storage capacitance to the total capacitance of the storage well 220 + bridge diffusion 205 + photodiode 200.

[0022] In practice, it is important to keep the charge injection substantially identical for each pixel. The charge injection can result from the raising of the voltage on the sample gate and to reset gates. Accurate control of the rise and fall times of the control signals can make sure that this charge injection stays constant.

[0023] An alternative embodiment is shown in Figure 3. Figure 3 shows a view of the wells of a single pixel during the integration time. In the Figure 3 embodiment, a photogate is used as the photoreceptor.

[0024] Both the photogate (PG) and the storage node 320 for the floating diffusion sense node (FD) have been reset. The storage node 320 is shown at the reset level in Figure 3.

[0025] N well 300 is located under a light shield 305, and the storage node 320 is isolated from the substrate by the N well, as in the embodiment of Figure 2. In this embodiment, the photogate 310 is connected to bridge diffusion 312. The value of the photogate may be reset by activating PMOS gate 315, to connect the bridge diffusion and photogate to the photogate reset well 318, which is held at the reset level Vr_{st}. Analogously, the storage node is reset by activating PMOS reset memory gate 325, bringing the storage node 320 to the reset level in storage node reset well 327.

[0026] This embodiment may use a photogate photoreceptor. The photogate allows charge to be collected over the same region as the photodiode pixel as described with reference to Figure 2. However, conversion gain may be increased in some situations by lowering the voltage on the photogate in order to force any charge that is present into the bridge diffusions during both the reset of the collection region and during sampling. This may compensate for the capacitance of the photoreceptor, which capacitance can actually be quite significant. Accordingly, the stored voltage can be considered as:

$$V_{stored} = V_{rst} - \frac{Q_{photons}}{C_{storage} + C_{bridge}}$$

[0027] This system may therefore increase conversion gain. However, the photogate may have a lower quantum efficiency than the photodiode. Therefore, any advantages of the second embodiment may be offset by quantum efficiency disadvantages.

[0028] Another embodiment shown in Figure 4 forms separated wells, a first well 400 for the photoreceptor 405 and a second well 430 for the readout circuit 435. This device is shown in charge integration mode, having lower positions corresponding to lower voltages. Holes may be integrated under the photogate 405 to form charge which is stored in one of the bridge diffusions 412 within the photo gate. The photogate is located in the first well 410. In this embodiment, the photogate may be reset within the first N well 410. The photogate is reset by activating the gate 408 to bring the photogate level to the reset level V_{rst} . This has the effect of clearing the charge within the photogate 405 as well as the bridge diffusions 412 and 414. An anti blooming gate 413 may also be located within the first well 410.

[0029] The output of the photogate is connected by a wire 420 to the bridge diffusion 414 within the second N well 430. The charge may be transferred. The value in the bridge diffusions

may also be transferred by the transfer gate 450 to the floating diffusion sensing node. The storage node 460 may be reset independently to the value in reset well 470 by activating the storage node reset gate 465.

[0030] In this embodiment, the gates are formed of P type MOS structures.

[0031] This pixel is operated in the same manner as the original photogate frame shutter, but with the signals converted to take into account the P type transistors. The conversion gain is:

$$V_{stored} = V_{rst} - \frac{Q_{photons}}{C_{storage}}$$

[0032] as in the above second embodiment, use of a photogate may reduce the quantum efficiency, and hence may offset some of the otherwise-obtained improvements.

[0033] Although only a few embodiments have been disclosed in detail above, other modifications are possible. For example, the photoreceptors as disclosed above could be other photoreceptor's besides the ones that are specifically disclosed. In addition, the sense of the semiconductor substrates, that is N type gates and P type gates could be

reversed. The N type well could of course be replaced by a P type well.

[0034] All such modifications are intended to be encompassed within the following claims, in which: